second read reference parameter, a third programming reference parameter and a third read reference parameter; and

sensing/program-verifying circuitry receiving a parameter which represents threshold voltage of one non-volatile memory cell, the first programming reference parameter, the first read reference parameter, the second programming reference parameter, the second read reference parameter, the third programming reference parameter and the third read reference parameter;

wherein the first read reference parameter is allocated between a level corresponding to the erase state and the first programming reference parameter, the second read reference parameter is allocated between the first programming reference parameter and the second programming reference parameter, and the third read reference parameter is allocated between the second programming reference parameter and the third programming reference parameter,

wherein the sensing/program-verifying circuitry generates data of at least two bits represented by the one non-volatile memory cell threshold voltage, verifies whether the one non-volatile memory cell threshold voltage is shifted to the threshold level indicating a selected one of the programming states, and programs the one non-volatile memory cell until it is verified that the one non-volatile memory cell threshold voltage has been shifted to that threshold level,

wherein the first programming reference parameter is used for verifying whether non-volatile memory cell threshold voltages are shifted to a first threshold level of the three threshold levels, the first read reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the first threshold level or to the threshold level indicating the erase state, and one of the first programming reference parameter and the first read reference parameter is shifted from and dependent upon the other,

wherein the second programming reference parameter is used for verifying whether non-volatile memory cell threshold voltages are shifted to a second threshold level of the three threshold levels, the second read reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the second threshold level or to the first threshold level, and one of the second programming reference parameter and the second read reference parameter is shifted from and dependent upon the other, and

wherein the third programming reference parameter is used for verifying whether non-volatile memory cell threshold voltages are shifted to a third threshold level of the three threshold levels, the third read reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the third threshold level or to the second threshold level, and one of the third programming reference parameter and the third read reference parameter is shifted from and dependent upon the other.

95.(New) A non-volatile semiconductor memory device according to claim 94,

wherein the parameter generating circuitry includes a first parameter generating circuit which generates the first programming reference parameter and the first read reference parameter, a second parameter generating circuit which generates the second programming reference parameter and the second read reference parameter, and a third parameter generating circuit which generates the third programming reference parameter and the third read reference parameter, and

wherein each of the first parameter generating circuit, the second parameter generating circuit and the third parameter generating circuit includes an element causing the corresponding one reference parameter and the corresponding other reference parameter to have different values.

96.(New) A non-volatile semiconductor memory device according to claim 95,

wherein each of the first parameter generating circuit, the second parameter generating circuit and the third parameter generating circuit further includes a reference cell which has substantially the same construction as each of said plurality of memory cells, and the reference cell and the element of each parameter generating circuit cooperate to provide a predetermined difference between the corresponding read and programming reference parameters.

97.(New) A non-volatile semiconductor memory device according to claim 94,

wherein each read reference parameter is dependent upon the corresponding programming reference parameter.

98.(New) A non-volatile semiconductor memory device according to claim 94,

wherein a conductivity value of the one non-volatile memory cell is decreased in order of the threshold level indicating the erase state, the first threshold level, the second threshold level and the third threshold level, and

wherein threshold voltages of non-volatile memory cells of one of a byte, a block and a chip level can be shifted to the threshold level indicating the erase state by an erase operation.

99.(New) A non-volatile semiconductor memory device according to claim 98,

wherein each of the plurality of non-volatile memory cells has a floating gate to which electrons are capable of being injected from a channel.

100.(New) A non-volatile semiconductor memory device according to claim 95,

wherein a conductivity value of the one non-volatile memory cell is decreased in order of the threshold level indicating the erase state, the first threshold level, the second threshold level and the third threshold level, and

wherein threshold voltages of non-volatile memory cells of one of a byte, a block and a chip level can be shifted to the threshold level indicating the erase state by an erase operation.

101.(New) A non-volatile semiconductor memory device according to claim 12,

wherein each of the plurality of non-volatile memory cells has a floating gate to which electrons are capable of being injected from a channel by hot electron injection.

102.(New) A non-volatile semiconductor memory device according to claim 96,

wherein a conductivity value of the one non-volatile memory cell is decreased in order of the threshold level indicating the erase state, the first threshold level, the second threshold level and the third threshold level, and

wherein threshold voltages of non-volatile memory cells of one of a byte, a block and a chip level can be shifted to the threshold level indicating the erase state by an erase operation.

103.(New) A non-volatile semiconductor memory device according to claim 102,

wherein each of the plurality of non-volatile memory cells has a floating gate to which electrons are capable of being injected from a channel.

104.(New) A non-volatile semiconductor memory device according to claim 5,

wherein a conductivity value of the one non-volatile memory cell is decreased in order of the threshold level indicating the erase state, the first threshold level, the second threshold level and the third threshold level, and

wherein threshold voltages of non-volatile memory cells of one of a byte, a block and a chip level can be shifted to the threshold level indicating the erase state by an erase operation.

105.(New) A non-volatile semiconductor memory device according to claim 104,

wherein each of the plurality of non-volatile memory cells has a floating gate to which electrons are capable of being injected from a channel.

106.(New) A non-volatile semiconductor memory device according to claim 94,

wherein the first, second and third read reference parameters are dependent upon the first, second and third programming reference parameters, respectively.--